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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GREGORY A MAJCHER, STEVEN P. BLECH, and
JOHN P. CASPERS

Appeal 2008-004809
Application 10/771,891
Technology Center 2100

Decided:[1] July 31, 2009

Before ALLEN R. MACDONALD, ST. JOHN COURTENAY III, and STEPHEN C. SIU, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 23-31 and 33-44, which are all of the claims remaining in this application. Claims 1-22 and 32 are cancelled. [2] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

Invention

Appellants' invention relates to industrial controllers. More particularly, the invention on appeal relates to providing an output value to an output device. (Spec. 1, ll. 11 and 12).

Claim 23 is illustrative:

> 23. A system that facilitates generating a dynamic output in a state machine, comprising:
>
> an input component that receives communications, the communication is related to at least one indicator that receives updated status/event information from the communication; and
>
> a logic function component that defines a logical function using at least one function block and links the logical function with the indicator to define the behavior of an output and selectively provide an output signal according to the logic function and the at least one indicator.

[2] We note that dependent claim 33 depends from cancelled claim 1.

Prior Art

The Examiner relies on the following references as evidence:

Tentij	US 6,513,129 B1	Jan. 28, 2003
Grieshaber	US 6,598,106 B1	July 22, 2003

Examiner's Rejections

I. Claims 23-28, 34, and 44 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Grieshaber.

II. Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Grieshaber.

III. Claims 29-31, 33, and 36-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Grieshaber in view of Tentij.

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs and the Answer for their respective details.

FINDINGS OF FACT

1. Grieshaber discloses a *recursive procedure* that constantly monitors the bus for errors or faults. (Col. 9, ll. 56-60).

2. The Examiner determined that each of the following teachings anticipates the claimed logic function: (1) every action of a modern computer, (2) "recursive procedures," and (3) a "Bus Hung" Yes/No decision process, (Fig. 7, ref. 704) (Ans. 11-12).

3. Grieshaber discloses that step 704 of Fig. 7 is a determination of whether or not a bus is hung. (Fig. 7 and col. 9, ll. 60-63)

4. Appellants' Specification states that "the *logic function* 118 may be defined in terms of one or more function blocks (not shown)

whereby a user may configure logical or other functions (*e.g.,* boolean operations, flip-flops, timer, counters, *and the like*)." (Spec. 9, ll. 22-24) (emphasis added).

5. Appellants' Specification states that "[t]he status/event *indicator* may comprise, for example, a list or table in module memory, whereby a processor in the module may update the information upon receipt of [a] network message, and may access the information in determining an output value in accordance with the user defined logic function." (Spec. 7, ll. 12-15, emphasis added).

APPELLANTS' CONTENTIONS

1. Appellants contend that the cited references fail to disclose or suggest the limitation of "a logic function component," as claimed (App. Br. 4-5 and Reply Br. 2-4).

2. Appellants further contend that the cited references fail to teach a logic function component that defines a logical function that is linked with an indicator to define the output behavior. (*Id.*).

ISSUES

Based upon our review of the administrative record, we have determined that the following issues are pivotal in this appeal:

1. Have Appellants shown that the Examiner erred in determining that the cited references disclose, teach, or suggest a "logic function," as claimed?

2. Have Appellants shown that the Examiner erred in determining that the claimed status/event indicator is merely data?

PRINCIPLES OF LAW

Anticipation

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. However, this is not an "ipsissimis verbis" test. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

Obviousness

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 419 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 417.

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the Examiner's proffered prima facie case.

ANALYSIS

102 rejection of claims 23-28, 34, and 44

We decide the question of whether Appellants have shown the Examiner erred in finding that Grieshaber discloses the limitations of a "logic function" and an "indicator," as recited in independent claims 23 and 44.

The Examiner relies on the teachings of Grieshaber and asserts: (1) that every action in a modern computer is a logic function, (2) that the "recursive procedures" as described in Grieshaber are logic functions as claimed (Ans. 11) and, (3) that the Yes/No "Bus Hung" decision process shown in Fig. 7, anticipates the claimed logic function. (Ans. 12; *see also* FF 2).

As a matter of claim construction, we note that the recited "logic function" is broadly defined in Appellants' Specification, as follows: "the logic function 118 may be defined in terms of one or more function blocks (not shown) whereby a user may configure logical or other functions (*e.g.,* boolean operations, flip-flops, timer, counters, *and the like*)." (FF 4.)

However, we note that independent claim 23 recites in pertinent part:

> a logic function component that defines a logical function using at least one function block and links the logical function with the indicator to define the behavior of an output and selectively provide an output signal according to the logic function and the at least one indicator.

(Claim 23; *see also* App. Br. 4).

Even given the breadth of Appellants' defined "logic function," it is our view that the Examiner's multiple readings of the claimed logical function component on different portions of the Grieshaber reference do not

clearly show how the aforementioned argued limitations are met, particularly the limitations of a logic function component that *defines a logical function* using at least one function block and *links* the logical function with the *indicator to define* the behavior of an output. (Claim 23).

While we agree with the Examiner's statement that every action in a modern computer is a logic function (Ans. 11), we find this general statement insufficient to meet each of the specific aforementioned argued limitations of claim 23, particularly the limitations of *linking* the logical function with the *indicator to define* the behavior of an output. (Claim 23).

We note that Appellants' Specification states that "[t]he status/event *indicator* may comprise, for example, a list or table in module memory, whereby a processor in the module may update the information upon receipt of [a] network message, and may access the information in determining an output value in accordance with the user defined logic function." (FF 5).

Regarding the claimed "indicator," the Examiner points to Grieshaber's Bus Fault Monitor 558, Monitor Processor 552, and Signal Processor 554 as functional blocks and the *signals* therebetween as indicators of faults (Ans 12, ¶2; *see also* Grieshaber, Fig. 5). However, we find Appellants contentions in the Reply Brief persuasive (with respect to claim 23) that "as claimed, an *indicator* is an entity that *receives* update status or event information from a communication received by an input component. Thus, the Examiner incorrectly points to a communication message between components as meeting the limitation of an indicator. A communication *signal* cannot *receive* update status or event information." (Reply Br. 3, ¶3, emphasis added).

Responsive to Appellants' argument, we broadly but reasonably construe the claimed "indicator" of claim 23 as a storage element that is capable of *receiving* status or event information, e.g., a list or table resident in memory.

Regarding the "recursive procedures," the Examiner states that "[o]ne of ordinary skill in the art, clearly understands this to be a logic function." (Ans. 11). However, we find the term "recursive procedure" (as used in Grieshaber) describes a repeated test for monitoring a bus for errors and/or faults and does not reasonably describe the claimed logical function component that defines a logical function using at least one function block that further *links* the logical function *with the indicator* to define the behavior of an output. (Claim 23). (FF 1).

Regarding the reference to step 704 of Fig. 7, we observe that step 704 is a decision of whether or not a bus is hung. (FF 3). Given our aforementioned construction of the claimed "indicator," we find the decision made at step 704 also does not anticipate the claimed logic function component that *defines a logical function* using at least one function block and *links* the logical function with the *indicator* to define the behavior of an output. (Claim 23).

Based on the record before us, Appellants have shown the Examiner erred in determining that Grieshaber discloses the claimed logic function component that *defines a logical function* using at least one function block and *links* the logical function with the *indicator* to define the behavior of an

output, as recited in claim 23. Accordingly, we reverse the Examiner's anticipation rejection of independent claim 23 as well as associated dependent claims 24-28 and 34.

Anticipation rejection of claim 44

In contrast to claim 23, we note that claim 44 is conspicuously silent regarding the previously argued limitations of *defining a logical function* using at least one function block and *linking* the logical function with the *indicator* to define the behavior of an output. (*See* App. Br. 4-5). Therefore, we find Appellants' arguments directed to claim 23 to be ineffective in demonstrating error in the Examiner's rejection of claim 44. (*Id.*).

Moreover, it is our view that the claimed "status" data (i.e., "means for determining the *status* of the associated logical function and status/event indicator components") is nonfunctional descriptive material that is not positively recited in the claim as performing any machine-implemented function. (App. Br. 4-5; claim 44) The *content* of nonfunctional descriptive material is not entitled to weight in the patentability analysis. *Cf. In re Lowry*, 32 F.3d 1579, 1583 (Fed. Cir. 1994) ("Lowry does not claim merely the information content of a memory . . . Nor does he seek to patent the content of information resident in a database."). *See also Ex parte Nehls* (BPAI Jan. 28, 2008), available at http://www.uspto.gov/web/offices/dcom/bpai/prec/fd071823.pdf; *Ex parte Curry,* 84 USPQ2d 1272 (BPAI 2005) (nonprecedential) (Fed. Cir. Appeal No. 2006-1003, aff'd Rule 36 Jun. 12, 2006); *Manual of Patent Examining Procedure* (MPEP) § 2106.01 (Eighth ed., Rev. 7, July 2008).

For at least the aforementioned reasons, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's prima facie case of anticipation regarding the rejection of independent claim 44.

103 rejection of claim 35

We consider next the Examiner's rejection of claim 35 as being unpatentable over the single reference Grieshaber. We note that claim 35 depends from claim 23 which was fully discussed *supra*. We do not find, nor does the Examiner establish, that any of the three teachings of Grieshaber that were previously discussed renders the specific limitations of base claim 23 obvious, i.e., "a logical function component that *defines a logical function* using at least one function block and *links* the logical function with the *indicator* to define the behavior of an output." (Claim 23). Accordingly, we reverse the Examiner's rejection of claim 35 for the same reasons discussed *supra* regarding independent claim 23.

103 rejection of claims 29-31

We consider next the Examiner's rejection of claims 29-31 as being unpatentable over Grieshaber in view of Tentij. We note that claims 29-31 also depend from claim 23, which was discussed *supra*. We do not find, nor does the Examiner establish, that Tentij cures any of the deficiencies of Grieshaber that were previously discussed. Accordingly, we reverse the Examiner's rejection of claims 29-31 for the same reasons discussed *supra* regarding independent claim 23.

103 rejection of claim 33

We consider next the Examiner's rejection of dependent claim 33 as being unpatentable over Grieshaber in view of Tentij.

We particularly note that claim 33 depends from cancelled claim 1 and is not argued separately in the Briefs (See note 2 above). Because Appellants have not shown the Examiner erred, we pro forma sustain Examiner's rejection of claim 33.

103 rejection of claims 36-43

We consider next the Examiner's rejection of claims 36-43 as being unpatentable over Grieshaber in view of Tentij. Appellants argue claims 36-43 as a group. We will, therefore, decide the appeal of these claims based upon representative claim 36. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants contend that the cited references fail to teach or suggest *transmitting the input to a logic function, the logic function contains at least one function block, associating the at least one indicator with the at least one function block, and providing an output based at least in part upon the at least one indicator and the logic function*, as recited by independent claim 36. (App. Br. 6).

Regarding claim 36, we observe that the claimed indicator here is not recited as *receiving* updated status/event information as was previously recited in claim 23. Therefore, we conclude that the scope of the claimed "indicator" of independent claim 36 is not limited to a structural element such as a table or list that is resident in memory. Here, we conclude that the scope of the recited "indicator" more broadly encompasses mere data.

(Claim 36). Because the scope of the claimed "indicator" may encompass data, we do not find persuasive Appellants' argument that neither Grieshaber nor Tentij teaches or suggests an association between an indicator and a function block and providing an output based in part on the indicator and the function block. (App. Br. 6). Moreover, given Appellants broad definition for the claimed "logical function" (FF 4), we disagree with Appellants' contention that determining a bus condition (as taught by Grieshaber) is not a logical function with at least one function block (App. Br. 6). Thus, we find the Examiner's arguments in the Answer persuasive when reconsidered in view of the broader scope of independent claim 36. (Ans. 11-13). Therefore, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's prima facie case of obviousness regarding representative claim 36. Accordingly, we sustain the Examiner's § 103 rejection of claim 36, and claims 37-43 that fall therewith, as being unpatentable over Grieshaber in view of Tentij.

CONCLUSIONS

Appellants have established that the Examiner erred in rejecting claims 23-28, and 34 under 35 U.S.C. § 102(e).

Appellants have not established that the Examiner erred in rejecting claim 44 under 35 U.S.C. §102(e).

Appellants have established that the Examiner erred in rejecting claims 29-31 and 35 under 35 U.S.C. § 103(a).

Appellants have not established that the Examiner erred in rejecting claims 33 and 36-43 under 35 U.S.C. § 103(a).

DECISION

The Examiner's decision rejecting claims 23-28, and 34 under 35 U.S.C. § 102(e) is reversed.

The Examiner's decision rejecting claim 44 under 35 U.S.C. §102(e) is sustained.

The Examiner's decision rejecting claims 29-31 and 35 under 35 U.S.C. § 103(a) is reversed.

The Examiner's decision rejecting claims 33 and 36-43 under 35 U.S.C. § 103(a) is sustained.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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